IN THE CLAIMS

1. (Currently Amended) A semiconductor chip comprising:

a plurality of outer edges;

a peripheral area located adjacent to the outer edges; and

a main circuit area located within the confines of the peripheral area, the main circuit area including integrated circuits,

wherein the peripheral area includes chip pads connected to the integrated circuits, a plurality of test pads electrically ~~being~~ connected to the integrated circuits for testing electrical properties of the integrated circuits, ~~the respective chip pads, the respective test pads,~~ the respective chip pads and test pads being arranged in ~~four~~ first and second pairs of rows at substantially uniform intervals, the first pair of rows being arranged substantially parallel to each other and the second pair of rows being arranged substantially parallel to each other, the first pair of rows being arranged substantially perpendicular to the second pair of rows, the chip pads being arranged in each of the rows adjacent the main circuit area of the semiconductor chip, and the test pads being located within each of the rows of chip pads, and the test pads ~~are~~ being substantially the same dimensional size as the chip pads.

2. (Cancelled)

3. (Cancelled)

4. (Currently Amended) The semiconductor chip of claim 1, wherein the test pads are located at the ends of each of the first and second pairs of rows of chip pads.

5. (Currently Amended) The semiconductor chip of claim 1, wherein the configuration of the main circuit area is arranged to form corners, and the test pads in each of the first and second pairs of rows are located near the corners of the main circuit area.

6. (Currently Amended) The semiconductor chip of claim 1, wherein the chip pads are arranged in rows parallel to at least one set of opposed outer edges of the semiconductor chip, and the test pads are arranged within each of the first and second pairs rows of chip pads.

7. (Currently Amended) The semiconductor chip of claim 1, wherein the test pads are arranged between chip pads within each of the first and second pairs rows of chip pads.

8. (Cancelled)

9. (Cancelled)

10. (Original) The semiconductor chip of claim 1, which comprises one of an edge-pad-type chip and a center-pad-type chip.

11. (Currently Amended) A tape carrier package comprising:

a semiconductor chip comprising a plurality of outer edges, a peripheral area located adjacent to the outer edges, and an main circuit area located within the confines of the peripheral area, the main circuit area including integrated circuits, the peripheral area including chip pads connected to the integrated circuits, and a plurality of test pads electrically connected to the integrated circuits for testing the electrical properties of the integrated circuits, the respective chip pads, the respective test pads, and the respective chip pads and test pads being arranged in ~~four~~ first and second pairs of rows at substantially uniform intervals, the first pair of rows being arranged substantially parallel to each other and the second pair of rows being arranged substantially parallel to each other, the first pair of rows being arranged substantially perpendicular to the second pair of rows, the chip pads being arranged in each of the rows adjacent the main circuit area of the semiconductor chip, and the test pads being located within each of the rows of chip pads, and the test pads ~~are~~ being substantially the same dimensional size as the chip pads; and

a tape wiring substrate.

12. (Cancelled)

13. (Cancelled)

14. (Currently Amended) The tape carrier package of claim 11, wherein the test pads are located at the ends of each of the first and second pairs rows of chip pads.

15. (Currently Amended) The tape carrier package of claim 11, wherein the configuration of the main circuit area is arranged to form corners, and the test pads in each of the first and second pairs of rows are located near the corners of the main circuit area.

16. (Currently Amended) The tape carrier package of claim 11, wherein the chip pads are arranged in rows parallel to at least one set of opposed outer edges of the semiconductor chip, and the test pads are arranged within each of the first and second pairs rows of chip pads.

17. (Currently Amended) The tape carrier package of claim 11, wherein the test pads are arranged between chip pads within each of the first and second pairs rows of chip pads.

18. (Cancelled)

19. (Original) The tape carrier package of claim 11, wherein the tape wiring substrate comprises an insulating base film, wiring patterns formed on the insulating base film, leads formed integrally with the wiring patterns, and dummy leads electrically isolated from the wiring patterns.

20. (Original) The tape carrier package of claim 19, which further comprises bumps connecting the chip pads to the corresponding leads and the test pads to the dummy leads.

21. (New) The semiconductor chip of claim 1, wherein the first pair of rows and the second pair of rows together form a rectangular configuration.

22. (New) The semiconductor chip of claim 11, wherein the first pair of rows and the second pair of rows together form a rectangular configuration.